REMARKS

Claims 25-35 are pending.

I. Claims 25, 26, 30, 32, 34 and 35 were rejected under 35 U.S.C. §103(a), as rendered obvious and unpatentable, over Takanashi et al. '939 in view of Tomita et al. '462, Hayashi et al. '039 and Onuma et al. '949 (*hereafter*: Takanashi, Tomita, Hayashi and Onuma). The Applicant respectfully traverses this rejection for the following reason(s).

A. Claim 25 calls for, in part, *a data bus connected to said computer, said data bus having a first data line for conveying input video data generated by said computer to said printing apparatus and a second data line for conveying dividing ratio data generated by said computer, and accompanying said input video data, to said printing apparatus.*

Of the applied art, Takanashi, Tomita, Hayashi and Onuma, it appears that the Examiner applies the apparent (as explained by the Examiner) teachings of Onuma's data bus for conveying data bits D1-D5 and D0, and Onuma's multiplexer 43 for storing the bit D0, with respect to the foregoing feature of claim 25. In so doing, the Examiner states "It would have been obvious at the time the invention was made to a person having ordinary skill in the art to implement the structural data bus as taught by Onuma et al. in the modified device of Takanashi et al."

The Examiner provides no reasons for making the obviousness statement. That is, the Examiner offers no basis of motivation which would have led the skilled artisan to utilize Onuma's data bus in the modified device of Takanashi (modified as suggested by the Examiner's application

of the apparent teachings of Tomita and Hayashi in paragraph 2 of pages 2 and 3 in Paper No. 45).

That a prior art device could be modified to produce the claimed device does not justify an obviousness rejection unless the prior art suggested the modification's desirability. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

It is insufficient that the prior art disclosed the components, either separately or used in other combinations, there must be some teaching, suggestion, or incentive to make the proposed combination. See *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 15 USPQ2d 1321 (Fed. Cir. 1990).

Therefore, a finding of a *prima facie* case of obviousness requires more than an indication that the elements are known to exist in the art. There must be some reason to combine references other than using the applicant's claims as a blueprint in an improper hindsight rejection.

Accordingly, the Examiner has not provided a *prima facie* basis of obviousness by setting forth clear supporting reasoning for suggesting that one of ordinary skill in the art would have further modified Takanashi's modified (modified as suggested by the Examiner's application of the apparent teachings of Tomita and Hayashi in paragraph 2 of pages 2 and 3 in Paper No. 45) device to include the data bus taught by Onuma.

In re Rijckaert, 28 USPQ2d 1955 (CAFC 1993) states:

> "A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell,* 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rhinehart,* 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976). If the examiner fails to establish a *prima facie* case, the rejection is improper and will be overturned. *In re Fine*, 837 F.2d

1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Considering the teachings of Onuma as understood by the Applicant, as compared to the Examiner's explanation, we find that the Examiner errs in his explanation of Onuma. The Examiner, **by omission**, appears to suggest that Onuma teaches *a data bus connected to said computer, said data bus having a first data line for conveying input video data generated by said computer to said printing apparatus and a second data line for conveying dividing ratio data generated by said computer, and accompanying said input video data, to said printing apparatus.* That is, the Examiner discusses, on page 4, "a first data line of the data bus" as conveying data bits D1-D5 and "second data line of the data bus" as conveying data bit D0 but **omits** discussing where the data bus originates, and **omits** what data bit D0 represents.

We note that the data bus conveying data bits D1-D5 and D0 originates at the output of a line buffer 2, and bits D0-D5 represent 6-bit digital tone data.

Accordingly, the " first data line of the data bus" conveying data bits D1-D5 is not disposed between the *computer* and the *printing apparatus*, nor is the "second data line of the data bus" conveying data bit D0 disposed between the *computer* and the *printing apparatus*. Additionally, the data bit D0 in Onuma is the least significant bit of the 6-bit digital tone data and not *dividing ratio data.*

Claim 25 requires *a first data line for conveying input video data generated by said computer to said printing apparatus and a second data line for conveying dividing ratio data generated by said computer, and accompanying said input video data, to said printing apparatus.*

Accordingly, it is not clear why the Examiner has applied Onuma in combination with the combination of applied art of Takanashi, Tomita and Hayashi. *See In re Sernaker*, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983) which states: "prior art references in combination do not make an invention obvious unless something in the prior art references would suggest the advantage to be derived from combining their teachings".

In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)

> One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.

B. Additionally, claim 25 requires *an output port connected to said second data line for receiving and storing said dividing ratio data.*

The Examiner erroneously indicates that Onuma's multiplexer 43 stores the bit D0.

Accordingly, by omission, the Examiner appears to suggest that Onuma's multiplexer 43 is equivalent to the claimed *output port connected to said second data line.* It should be noted here that claim 25 also requires *a second divider for generating a second clock signal by dividing said pulses of said local clock signal in dependence upon the stored dividing ratio data, the stored dividing ratio data being output from said output port .*

We find no teaching in Onuma that multiplexer 43 stores the data bit D0, nor any teaching that the data bit D0 be output from multiplexer 43 to be applied to a divider. Note that Onuma discloses that multiplexer 43 provides an output to timing circuit 44, which in turn, transfers the output signal of the multiplexer 43 to the recording head 1.

According to the Examiner's failure to establish a *prima facie* basis of obviousness, the rejection of claim 25 is deemed to be in error and should be withdrawn.

C. In further analysis of the Examiner's rejection, the primary reference applied against the claimed invention is Takanashi. In applying Takanashi, the Examiner **initially** refers us to col. 2, lines 50-56 which provide a description with respect to FIG. 1, a prior art apparatus (prior to Takanashi's invention), that functions to drive a linear array 11 of LEDs. The linear array 11 of the LEDs corresponds to one horizontal line, and the LEDs correspond to pixels respectively. The prior art apparatus of FIG. 1 includes a driver 12, a corrective ROM (read-only memory) 13, an address counter 14, a conversion ROM 15, a serial-to-parallel (S/P) converter 16, a latch 17, and a chopper generator 18.

Then, the Examiner refers us to a plurality of clock signals of different phases (CLKa-CLKC, Figs. 5-6) that can be selected (selector 120) in accordance with data received and separated from input data (DIN0 and DIN1).

The Examiner fails to explain how the plurality of clock signals of different phases (CLKa-CLKC, Figs. 5-6) that can be selected (selector 120) in accordance with data received and separated from input data (DIN0 and DIN1) relate to Takanashi's Fig. 1. That is, it is not understood why the Examiner chooses to discuss the prior art apparatus of Takanashi's Fig. 1 (not a part of Takanashi's invention), and then chooses to discuss part of Takanashi's invention related to Figs. 5 and 6.

The Examiner cannot pick and choose among the individual elements of assorted prior art references to recreate the claimed invention. *See, e.g., Azko N.V. v. United States Int'l Trade*

Comm'n, 808 F.2d 1471, 1481, 1 USPQ2d 1241, 1246 (Fed. Cir. 1986), cert. denied , 107 S.Ct. 2490 (1987).

The Examiner then goes on to discuss what Takanashi fails to teach, *i.e.,* "first and second dividers for generating first and second signals by dividing the initial clock by a predetermined ratio different from each other, as well as the chopping unit comprising AND gate (instead of NAND and NOR gates as disclosed in Fig. 5)."

Takanashi discloses that "FIG. 5 shows an essential part of a second embodiment of this invention which is similar to the embodiment of FIGS. 3 and 4 except for the following design changes. The second embodiment includes a pulse width modulator 100 which replaces the combination of a comparator 6 and a flip-flop 7 in each processing unit 1. In addition, a first counter 30 and a second counter 32 are provided other than each processing unit 1 and used in common for the respective processing units 1."

We note here that there are no NOR gates illustrated in Fig. 5, however, comparators 122 and 124 of Fig. 5 do include NOR gates as illustrated in Figs. 7 and 8.

There is no disclosure in Takanashi that relates the chopping unit 18 of Fig. 1 to any component of Fig. 5. Accordingly, the Examiner's mentioning of "the chopping unit" in the discussion of what Takanashi fails to teach, and the discussion of Takanashi's col. 2, lines 50-56, erroneously suggest that Fig. 1 of Takanashi is related to Takanashi's Fig. 5. To the contrary, Takanashi fails to suggest combining any of the elements of Figs. 1 and 5.

D. As noted above, the Examiner indicates that Takanashi fails to teach, *i.e.,* "first and second

dividers for generating first and second signals by dividing the initial clock by a predetermined ratio different from each other, as well as the chopping unit comprising AND gate (instead of NAND and NOR gates as disclosed in Fig. 5)." Up to this point in the rejection, prior to the discussion of Tomita, Hayashi and Onuma, we find no discussion by the Examiner of the features of:

> *a data bus connected to said computer, said data bus having a first data line for conveying input video data generated by said computer to said printing apparatus and a second data line for conveying dividing ratio data generated by said computer, and accompanying said input video data, to said printing apparatus;*
>
> *an output port connected to said second data line for receiving and storing said dividing ratio data;*
>
> *a clock signal generator for generating a local clock signal exhibiting a plurality of pulses characterized by a first frequency;*
>
> *a data transmitter for converting said input video data into serial video data in response to said first clock signal, and for transmitting said serial video data in response to a horizontal synchronization signal;*
>
> *a print controller for generating beam data in response to said chopped serial video data; and*
>
> *a laser beam generator for generating a scanning laser beam for defining images corresponding to said beam data, and generating a beam detection signal derived from the scanning of said scanning laser beam; and*
>
> *said print controller generating said horizontal synchronizing signal in response to said beam detection signal*

as required by claim 25.

Accordingly, the Examiner's discussion of what Takanashi fails to teach, *i.e.,* "first and second dividers for generating first and second signals by dividing the initial clock by a predetermined ratio different from each other, as well as the chopping unit comprising AND gate (instead of NAND and NOR gates as disclosed in Fig. 5)," appears to suggest that the foregoing features of claim 25 can be found in Takanashi. However, the Examiner must point out where the foregoing features are found in Takanashi in order to satisfy the requirement that the PTO establish

a *prima facie* basis of obviousness. Note, *Ex parte Levy*, 17 USPQ2d 1461, 1462 (1990) states:

> "it is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference."

Accordingly, it is the Applicant's contention that Takanashi not only fails to teach "first and second dividers for generating first and second signals by dividing the initial clock by a predetermined ratio different from each other, as well as the chopping unit comprising AND gate (instead of NAND and NOR gates as disclosed in Fig. 5)," but also fails to teach:

> *a data bus connected to said computer, said data bus having a first data line for conveying input video data generated by said computer to said printing apparatus and a second data line for conveying dividing ratio data generated by said computer, and accompanying said input video data, to said printing apparatus;*
>
> *an output port connected to said second data line for receiving and storing said dividing ratio data;*
>
> *a clock signal generator for generating a local clock signal exhibiting a plurality of pulses characterized by a first frequency;*
>
> *a data transmitter for converting said input video data into serial video data in response to said first clock signal, and for transmitting said serial video data in response to a horizontal synchronization signal;*
>
> *a print controller for generating beam data in response to said chopped serial video data; and*
>
> *a laser beam generator for generating a scanning laser beam for defining images corresponding to said beam data, and generating a beam detection signal derived from the scanning of said scanning laser beam;* and
>
> *said print controller generating said horizontal synchronizing signal in response to said beam detection signal*

as required by claim 25.

Accordingly, the rejection of claim 25 is deemed to be in error and should be withdrawn.

Of the foregoing, it appears, as discussed previously with respect to Onuma as applied by the

Examiner, that not only does Takanashi fail to teach "first and second dividers for generating first and second signals by dividing the initial clock by a predetermined ratio different from each other, as well as the chopping unit comprising AND gate (instead of NAND and NOR gates as disclosed in Fig. 5)," but also fails to teach:

> *a data bus connected to said computer, said data bus having a first data line for conveying input video data generated by said computer to said printing apparatus and a second data line for conveying dividing ratio data generated by said computer, and accompanying said input video data, to said printing apparatus;* and
> *an output port connected to said second data line for receiving and storing said dividing ratio data;*

Additionally, as discussed above in section **A**, since Onuma fails to teach the foregoing features, then the rejection is deemed to be in error, and should be withdrawn.

E. In view of the Examiner's discussion of Takanashi's Fig. 5, we note that in Takanashi an image signal DATA is fed to a shift register 2 (Fig. 3), and is stored into the shift register 2. The shift register 2 includes a series combination of storage sections corresponding to pixels respectively. The shift register 2 has a capacity corresponding to the product of the number of pixels and the bit number "n" of the image signal DATA, that is, a capacity for storing a 1-line quantity of the image signal DATA.

Each of the storage sections of the shift register 2 are respectively connected to processing units 1 in Fig. 3, however, with respect to Fig. 5, a first counter 30 and a second counter 32 are provided other than counter 4 of each processing unit 1 and used in common for the respective processing units 1. Also, a pulse width modulator 100 replaces the combination of a comparator 6

and a flip-flop 7 in each processing unit 1.

The pulse width modulator 100 includes a selector 120, comparators 122 and 124, a flip-flop 126, NAND gates 130, 134, and 136, and a NOT gate 132. The selector 120 receives four-phase clock signals CLKA, CLKB, CLKC, and CLKD which have a predetermined timing relation with each other as shown in FIG. 9(A). Specifically, the clock signals CLKA-CLKD are out of phase with each other by values corresponding to a half of a 1-pulse width. The clock signals CLKA-CLKD are fed from a known clock signal generator (not shown). Image data fed from a latch 5 (see FIG. 3) have eight bits DIN0-DIN8. The selector 120 receives the two lower bits DIN0 and DIN1 of the image data. The selector 120 selects one of the clock signals CLKA-CLKD in response to the two lower bits DIN0 and DIN1 of the image data, and transmits the selected clock signal Z to a T terminal of the flip-flop 126.

There is no teaching in Takanashi of *conveying dividing ratio data generated by said computer, and accompanying said input video data, to said printing apparatus*, and no teaching of *an output port connected to said second data line for receiving and storing said dividing ratio data.*

Following the Examiner's discussion of Takanashi, the Examiner applies Tomita, and discusses Tomita's AND gate circuit 3 with respect to the claimed *chopping unit for receiving said serial video data transmitted by said data transmitter, and in response to said second clock signal, generating chopped serial video data*, and then discusses the teachings of Hayashi.

The Examiner refers us to Tomita's pulse signal selection circuit 7, which applies strobe signals STB1 through STBN to the AND gates of chopping unit 3, with which Tomita teaches changing the power level of a light emitting diode, and further refers us to Hayashi's teaching of

changing a power level of a light source in an electrophotographic apparatus in accordance with environmental conditions.

Additionally, the Examiner suggests that the pulse selection signal applied to the pulse signal selection circuit 7 to be the claimed *dividing ratio data generated by said computer, and accompanying said input video data, to said printing apparatus* by "broadly" interpretating Tomita.

Tomita discloses that the "pulse signal selecting circuit 7 selectively outputs one or more N strobe signals STB1 through STBN generated by a pulse signal generating circuit 6, in accordance with a pulse selection signal supplied from the external circuit (not shown) such as the aforementioned CPU." Additionally, Tomita discloses that the"shift register 4 converts pixel data in serial form into pixel data in parallel form by using a shift clock supplied from an external circuit (not shown) such as a central processing unit provided in a printing machine, for example."

Accordingly, Tomita clearly teaches that the "external circuit" is a component of the "printing machine" and is preferably a CPU of the printing machine. Therefore, Tomita can only be interpreted as broadly as allowed by the limitations set forth in Tomita, and the limitation that the "external circuit" that provides the pulse selection signal to the pulse selection circuit 7 is limited to a component of the printing machine, thereby eliminating any suggestion that the *dividing ratio data* be generated by a computer, *and accompanying said input video data, to said printing apparatus.* There is no teaching in Tomita which would permit the broad interpretation as made by the Examiner.

Therefore, the combination of Tomita and Hayashi fail to teach modification of Takanashi in order to render a device having *a data bus connected to said computer, said data bus having a*

first data line for conveying input video data generated by said computer to said printing apparatus and a second data line for conveying dividing ratio data generated by said computer, and accompanying said input video data, to said printing apparatus; an output port connected to said second data line for receiving and storing said dividing ratio data; and *a second divider for generating a second clock signal by dividing said pulses of said local clock signal in dependence upon the stored dividing ratio data, the stored dividing ratio data being output from said output port.*

According to the Examiner's fails to establish a *prima facie* basis of obviousness, the rejection of claim 25 is deemed to be in error and should be withdrawn.

F. We note that the combined teachings of Tomita and Hayashi would suggest changing the power level of the light emitting diodes (LEDs) in Tomita based on environmental conditions as taught by Hayashi. The change in power level is a result of pulse duration, *i.e.,* pulse width, of a signal applied to the LEDs by controlling the on/off time of Tomita's AND gates.

We note also, that there has been no showing that efficiency of Takanashi's apparatus is subject to environmental conditions. Additionally, we note that data being provided to the LEDs in Takanashi are already pulse width modified by Takanashi's the pulse width modulator 100 (Fig. 5).

The Examiner's suggestion of combining Tomita's AND gate circuit chopping means and pulse signal generating circuit with Takanashi's apparatus lacks any suggestion of how such a combination would be achieved, and lacks any showing of results that may be achieved based on such a combination. That is, the Examiner leaves it up to the Applicant to determine whether

Tomita's **pulse width modulation circuit**, *i.e.*, AND gate circuit chopping means and pulse signal generating circuit, would replace Takanashi's the pulse width modulator 100, be placed before Takanashi's the pulse width modulator 100 or be placed after Takanashi's the pulse width modulator 100.

However, the burden is on the Examiner to establish a *prima facie* case of obviousness, which the Examiner fails to do because it is not clear how the proposed modification of Takanashi would be achieved.

Additionally, there has been no showing that any modification of Takanashi by utilizing Tomita's pulse width modulation circuit would result in a device that still functions in a manner as desired by Takanashi. Without any showing of how the proposed combination would be achieved, the Applicant is prevented from presenting evidence that the may support a showing that such a modification would destroy the intended purpose of Takanashi's device such that it would no longer be able to function as intended, since such destruction is an important indication of non-obviousness, see *In re Gordon,* 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

According to the Examiner's fails to establish a *prima facie* basis of obviousness, the rejection of claim 25 is deemed to be in error and should be withdrawn.

SUMMARY

It has been shown that the proposed combination of references fail to teach

> *a data bus connected to said computer, said data bus having a first data line for conveying input video data generated by said computer to said printing apparatus and a second data line for conveying dividing ratio data generated by said*

computer, and accompanying said input video data, to said printing apparatus;

an output port connected to said second data line for receiving and storing said dividing ratio data; and

a second divider for generating a second clock signal by dividing said pulses of said local clock signal in dependence upon the stored dividing ratio data, the stored dividing ratio data being output from said output port.

as set forth in claim 25, thus claim 25 is deemed to be non-obvious in view of the applied art.

Additionally, it has been argued that Takanashi differs from claim 25 in also failing to teach any of the following features of claim 25.

a data transmitter for converting said input video data into serial video data in response to said first clock signal, and for transmitting said serial video data in response to a horizontal synchronization signal;

a print controller for generating beam data in response to said chopped serial video data; and

a laser beam generator for generating a scanning laser beam for defining images corresponding to said beam data, and generating a beam detection signal derived from the scanning of said scanning laser beam; and

said print controller generating said horizontal synchronizing signal in response to said beam detection signal.

Since Tomita, Hayashi and Onuma were not applied with regard to the foregoing features of claim 25, then the rejection is deemed to be in error for failure to show that all the features of claim 25 are taught by the applied art.

Further, apparatus claim 30 is similar to claim 25 and is deemed to be non-obvious for the same reasons as argued above with respect to claim 25. Likewise, claim 34 calls for *conveying dividing ratio data, generated by said data source, to said electrophotographic developing type reproduction apparatus over said data bus connected to said data source; separating said dividing*

ratio data from said input video data; storing the dividing ratio data, separated from said input video data, in memory; and *generating a second clock signal by dividing said pulses of said local clock signal in dependence upon the dividing ratio data output from said memory*, wherein the foregoing features are similar to the features noted above as lacking in teachings of the proposed combination of applied references. Therefore, claim 34 is deemed to be non-obvious for the same reasons as argued above with respect to claim 25. Additionally, claim 34 calls for *generating beam data in response to said chopped serial video data; generating a scanning laser beam for defining images corresponding to said beam data, and generating a beam detection signal derived from the scanning of said scanning laser beam;* and *generating said horizontal synchronizing signal in response to said beam detection signal*, wherein the foregoing features are similar to the features noted above as lacking in Takanashi, and wherein Tomita, Hayashi and Onuma were not applied with regard to these features. Thus, the rejection of claim 34 is deemed to be in error for failure to show that all the features of claim 34 are taught by the applied art.

Accordingly, the rejection of claims 25, 26, 30, 32, 34 and 35 is deemed to be in error and should be withdrawn.

II. Claims 27-29, 31 and 33 were rejected under 35 U.S.C. §103(a), as rendered obvious and unpatentable, over the proposed combination of Takanashi, Tomita, Hayashi and Onuma as applied to claims 25, 30 and 34 and in further view of Wiklof et al '399 (*hereafter*: Wiklof). The Applicant respectfully traverses this rejection for the following reason(s).

A. The Examiner has applied Wiklof to the proposed combination of Takanashi, Tomita, Hayashi and Onuma, wherein Wiklof teaches which allowing a thermal printer 20 to be controlled and adjusted by a user.

Wiklof was not applied with respect to any of the features set forth in claims 25, 30, and 34 noted in section **I,** above, as lacking in the teachings of Takanashi, Tomita, Hayashi and Onuma. Accordingly, claims 27-29, 31 and 33 are deemed to be non-obvious for the same reasons as claims 25, 30 and 34.

B. Additionally, we note that claim 25 (and similarly claims 30 and 34) calls for *a first divider for generating a first clock signal by dividing pulses of said local clock signal, said first clock signal having a plurality of pulses characterized by a second frequency different from said first frequency;* and *a second divider for generating a second clock signal by dividing said pulses of said local clock signal in dependence upon the stored dividing ratio data, the stored dividing ratio data being output from said output port, said second clock signal having a plurality of pulses characterized by a third frequency different from said first and second frequencies and established in dependence upon said stored dividing ratio data.*

Claims 27-29, 31 and 33 call for changing the enabling a user to change a characteristic of the *second clock signal.* The Examiner has not provided a *prima facie* basis of obviousness to support the changing of a characteristic of such *said second clock signal*, and has not even identified which signal in the proposed modification of Takanashi corresponds to such *said second clock signal.* Instead, the Examiner merely suggest modification by incorporating Wiklof's "selecting mode

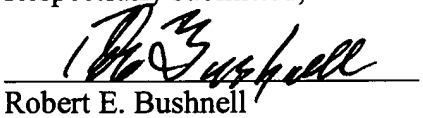
for enabling user selection."

Accordingly, the Examiner's fails to establish a *prima facie* basis of obviousness, the rejection of claims 27-29, 31 and 33 is deemed to be in error and should be withdrawn.

The examiner is respectfully requested to reconsider the application, withdraw the objections and/or rejections and pass the application to issue in view of the above amendments and/or remarks.

Should a Petition for extension of time be required with the filing of this Response, the Commissioner is kindly requested to treat this paragraph as such a request and is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of the incurred fee if, **and only if**, a petition for extension of time be required **and** a check of the requisite amount is not enclosed.

Respectfully submitted,



Robert E. Bushnell
Attorney for Applicant
Reg. No.: 27,774

1522 K Street, N.W.
Washington, D.C. 20005
(202) 638-5740

Folio: P53706
Date: 1/9/04
I.D.: REB/MDP